Time: 3 hours

2007 JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY

II B.TECH I SEMESTER REGULAR EXAMINATIONS PULSE AND DIGITAL CIRCUITS (COMMON TO ELECTRICAL & ELECTRONIC ENGINEERING, ELECTRONICS & COMMUNICATION ENGINEERING, ELECTRONICS & INSTRUMENTATION ENGINEERING AND ELECTRONICS & TELEMATICS)

NOVEMBER 2007

	Max Marks: 80
	Answer any FIVE Questions All Questions carry equal marks
1	(a) Verify $V^2 = (V/2)(e^2x+1) = (V/2)$ tanks for a symmetrical square wave applied to a low
1.	pass RC circuit.
(b)	Derive the expression for percentage tilt(P) of a square wave output of RC high pass circuit.
	[8+8]
2. ((a) Give the circuits of different types of shunt clippers and explain their operationwith the help of
the	ir transfer characteristics.
(b)	Draw the diode differentiator comparator circuit and explain the operation of it when ramp input
sig	nal is applied. [8+8]

3. Write Short notes on:

(a) Diode switching times

(b) Switching characteristics of transistors

(c) FET as a switch. [4+8+4]

4. (a) Draw the circuit diagram of a Schmitt trigger circuit and explain its operation. Derive the Expressions for its UTP and LTP.

(b) Explain how an Schmitt trigger circuit acts as a comparator. [12+4]

5. (a) Explain the basic principles of Miller and bootstrap time base generators.

(b) A transistor bootstrap ramp generator is to produce a 15V, 5ms output to a 2kohms load resistor. The ramp is to be linear within 2%. Design a suitable circuit using Vcc = 22V, -VEE = -22V and transistor with hfe(min) = 25. The input pulse has an amplitude of -5V, pulse width = 5ms and space width = 2.5ms. [8+8]

6. (a) What is relaxation oscillator? Name some negative resistance devices used as relaxation oscillators and give its applications.

(b) With the help of a circuit diagram and waveforms, explain the frequency division by an astable multivibrator? [8+8]

7. (a) Why are sampling gates called linear gates?

- (b) What are the other names of a gate signal?
- (c) Compare the unidirectional and bi-directional sampling gates.
- 8. (a) Why totem pole is used in DTL? Draw the circuit diagram and explain a DTL gate with this.

<text><text>