Sl. No. 33205 A–FTF–J–FFB

इन्जीनियरिंग सेवा परीक्षा, ...
Engineering Service Examination.

ELECTRICAL ENGINEERING

Paper—II

(Conventional)

Time Allowed : Three Hours	Maximum Marks : 200

INSTRUCTIONS

Candidates should attempt FIVE questions in all.

Question No. 1 is compulsory. The remaining FOUR questions are to be attempted by selecting ONE question each from Sections A, B, C and D.

The number of marks carried by each question is indicated at the end of the question.

Answers must be written in ENGLISH.

Assume suitable data, if necessary and indicate the same clearly.

Wherever a question is attempted, all its subdivisions must be attempted.

Unless otherwise indicated, symbols and notations have their usual meanings.

1. (A) Choose and write the correct answer : 2×10=20

(a) When a 2300/230 volts, 50 kVA, 50 Hz transformer is connected as an autotransformer to supply a 2300 V circuit from a 2530 V source, the kVA rating of the auto-transformer will be

(i) 550 kVA

(ii) 500 kVA

(iii) 450 kVA

(iv) 50 kVA

(b) The terminal voltage of a d.c. shunt motor is halved and the load torque is varied as the square of the speed, the field flux remaining constant. Consequently the armature current would be approximately

(i) constant

(ii) halved

(iii) one-fourth of the normal value

(iv) twice the normal value

(c) HVDC monopolar link uses

(i) one conductor usually of negative polarity

(ii) one conductor usually of positive polarity

(iii) two conductors, one of positive and the other of negative polarity

(iv) two conductors both of negative polarity

(d) The surge impedance of a 3-phase, 400 kV transmission line is 400 Ω. The surge impedance loading (SIL) is

(i) 400 MW

(ii) 1600 MW

(iii) 400 kW

(iv) 200 MW

(e) In a *J-K* flip-flop, race-around condition occurs when

(i) both J and K inputs are 0

(ii) both J and K inputs are 1

(iii) $J = 1$ and $K = 0$

(iv) $J = 0$ and $K = 1$

(f) A single instruction to clear the lower four bits of the accumulator in 8085 microprocessor is

(i) XRI 0FH

(ii) ANI F0H

(iii) XRI F0H

(iv) ANI 0FH

(g) In microprocessor-based systems, DMA facility is required to

(i) increase the speed of data transfer between the microprocessor and the I/O devices

(ii) increase the speed of data transfer between the microprocessor and the memory

(iii) increase the speed of data transfer between the memory and the I/O devices

(iv) improve the reliability of the system

(h) The signal to noise ratio of one communication link is 60 dB. If three such identical links are used in tandem, the overall signal to noise ratio is

(i) 180 dB

(ii) 64·77 dB

(iii) 55·23 dB

(iv) 20 dB

(i) In a sinusoidal PWM inverter, the harmonics are of the form $kp \pm l$ (p is the carrier ratio) where

(i) both k and l are either even or both are odd

(ii) k is always even and l is always odd

(iii) k is always odd and l is always even

(iv) k is odd and l is even or k is even and l is odd

(j) As a consequence of low internal generation in a GTO, it has

(i) an increased latching current value

(ii) an increased holding current value

(iii) both increased holding and latching currents

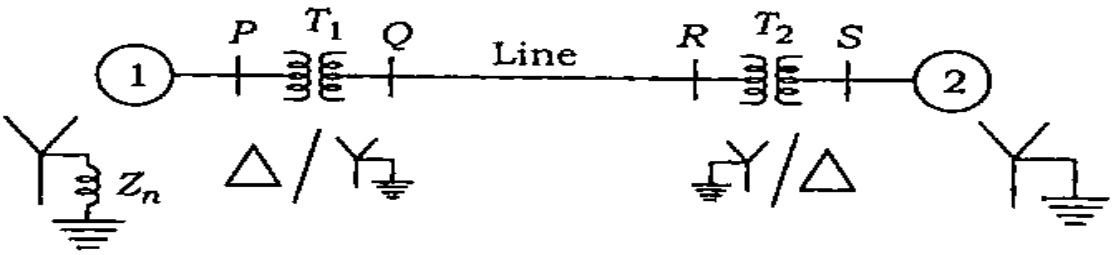
(iv) increased holding current and decreased latching current

(B) Answer the following questions : 4×5=20

(a) The analysis of magnetic circuit is simplified by making an analogy between magnetic and d.c. resistive circuits, wherein ϕ, the flux through the magnetic circuit is considered analogous to I, the current through

the electric circuit; apart from analogies between other magnetic and electric circuit quantities. Identify differences between the two circuits in so far as the through variables ϕ and I are concerned.

(b) One-line diagram of a small power system is given below. Draw the zero-sequence network.



The zero-sequence reactances of the various components are denoted as follows :

Generator 1 = X_{10}

Generator 2 = X_{20}

Line = X_{L0}

Transformer T_1 = X_{t10}

Transformer T_2 = X_{t20}

(c) Implement the function

$$F(W, X, Y, Z) = \Sigma m\,(0, 1, 3, 4, 8, 9, 15)$$

using an 8 : 1 multiplexer.

(d) For the 8085-based micro-computer, define stack and stack pointer, and describe their uses.

(e) Draw the circuit diagram and waveform of load voltage and current of two-stage sequence control of single-phase a.c. voltage regulator feeding resistive load. Assume 1 : 1 transformers are used on the source side. Give sequence of operation of two regulators when voltage control is required from 0 to V and V to $2V$.

Section—A

2. (a) A coil wound on a magnetic core is excited by the following voltage sources :

(i) 100 V, 50 Hz

(ii) 110 V, 60 Hz

Compare the hysteresis losses and eddy-current losses with these two different sources. For hysteresis loss, consider Steinmetz constant $n = 2$. 8

(b) Identify various losses that occur in the shunt d.c. machine.

A d.c. machine is connected across a 240 V line. It rotates at 1200 r.p.m. and is generating 230 volts. The armature current is 40 amperes.

(i) Is the machine functioning as a generator or as a motor?

(ii) Find the resistance of the armature circuit.

(iii) Determine the electromagnetic torque.

(iv) If the load is thrown off, what will be the generated voltage and the speed of the machine, assuming that there is negligible effect of armature reaction? 12

(c) Draw the open-circuit characteristic and short-circuit characteristic of synchronous machine, and show the variation of synchronous impedance, Z_s, with the field current, I_f. Explain the nature of variation of Z_s.

A 3-phase, Y-connected synchronous generator rated at 10 kVA and 230 V has a synchronous reactance of 1·2 ohms per phase and an armature resistance of 0·5 ohm per phase. Calculate the following : 20

(i) The % voltage regulation at full load with 0·8 lagging power factor

(ii) The power factor of the load such that the voltage regulation is zero on full load

3. (a) State and explain the conditions required for the successful parallel operation of single-phase transformers.

A single-phase load is supplied through a 34·5 kV feeder and a 34·5/2·4 kV transformer. The feeder has an

impedance of $50 + j80$ ohms and the transformer has an equivalent impedance of $24 + j120$ ohms referred to its high-voltage side. The load takes 260 kW at 2·3 kV and 0·866 lagging power factor.

(i) Find the voltage at the primary side of the transformer.

(ii) Determine the voltage at the sending end of the feeder.

(iii) Calculate the real and reactive power inputs at the sending end of the feeder. 20

(b) Give methods for starting of 3-phase squirrel-cage induction motors.

A 3-phase, 400 V, 100 kW, 50 Hz, 6-pole induction motor operates at 3% slip at full load. Determine the following : 15

(i) The speed of the motor and its direction relative to the rotating magnetic field

(ii) The rotor frequency

(iii) The speed of the stator field

(iv) The speed of the air-gap field

(v) The speed of the rotor field relative to stator rotating field

(c) Give reasons why a single-phase induction motor has poorer performance as compared to a 3-phase induction motor. 5

Section—B

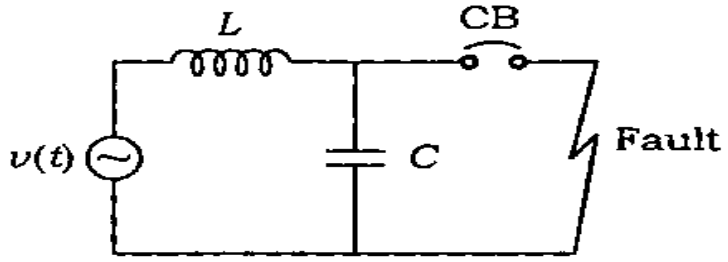
4. (a) A 50 Hz, 3-phase transmission line is 200 km long. It has a total series impedance of $35 + j140\ \Omega$ and a shunt admittance of $930 \times 10^{-6} \angle 90°$ ℧. It delivers 40 MW power at 220 kV with 0·9 power factor lagging. Find the magnitude of the sending-end voltage. Consider nominal-π model of the line. 20

(b) A 3-phase, 50 Hz generator is rated at 500 MVA, 20 kV with $X_d'' = 0 \cdot 2$ per unit. It supplies purely resistive load of 400 MW at 20 kV. The load is connected directly across the terminals of the generator. If all the three phases of the load are short circuited simultaneously, find the initial symmetrical r.m.s. current in the generator in per unit on a base of 500 MVA, 20 kV. 5

(c) A 50 Hz, 3-phase generator is supplying 60% of P_{max} to an infinite bus through a reactive network. A fault occurs which increases the reactance of the network between the generator internal voltage and the infinite bus by 400%. When the

fault is cleared, the maximum power that can be delivered is 80% of the original maximum value. Determine the critical clearing angle for the condition described. 15

5. *(a)* A single-phase equivalent circuit for studying the transient recovery voltage when a CB clears a fault is given below. Compute average value of rate of rise of restriking voltage (RRRV). 10



$$v(t) = 11000\cos 314t \text{ volts}$$

$$L = 1 \text{ mH}, \; C = 400 \text{ pF}$$

(b) A surge of 10 kV magnitude travels along a cable towards its junction with an overhead line. The inductance and capacitance of the cable and overhead line are respectively 0·3 mH, 0·4 μF and 1·5 mH, 0·012 μF per km. Find the voltage rise at the junction due to the surge. 10

(c) Explain Gauss-Seidel iterative method for solving Load Flow Equations. 20

Section—C

6. *(a)* A monostable multivibrator is to be constructed using an opamp. Draw the circuit diagram of the multivibrator for generating a positive pulse and explain its working with the help of waveforms. Derive an expression for the period of the pulse in terms of the circuit parameters. 16

(b) Show how *n*-channel enhancement MOSFETs can be connected to obtain *(i)* NOR logic and *(ii)* NAND logic. Verify the logical operation in each case. 8

(c) Design a mod-6 counter to go through the sequence of states as given in the table below using *S-R* flip-flops :

Sequence No.	*Required State Sequence*	
0	0 0 0	
1	0 1 0	
2	0 1 1	
3	1 1 0	
4	1 0 1	
5	0 0 1	→ Repeat from 0 0 0

Show the state table indicating the present state, the next state for each present state along with the input requirements of each of the *S* and *R*

inputs. Show clearly the minimization of logic requirements using K-maps. Write the logical expressions for each excitation input of all the flip-flops. Draw the logic diagram of the counter designed by you. 16

7. *(a)* In 8085 microprocessor, there are 3 sets of communication lines, called buses. Which are they? Explain each of them in brief. 12

(b) The memory location 2050 holds the data byte F7H. Write instructions to transfer the data byte to the accumulator using 3 different opcodes MOV, LDAX and LDA. Also show the register contents for all 3 opcodes. After examining all of them, find which method is more efficient by giving your comments. 12

(c) A set of 12 voltage readings is stored in memory locations 2070H to 207BH. The readings are expected to be positive and less than 100_{10}. Write a program to—

(i) check each reading to determine whether it is positive or negative;

(ii) reject all negative readings;

(iii) add all positive readings;

(iv) output FFH to port 1 at any time, when the sum exceeds FFH to represent overflow, otherwise, display the sum.

If no output port is available in the system, then store FFH in memory location 2090H, when the sum exceeds FFH, otherwise, store the sum in memory location 2090H. Write comments for each instruction. 16

Section—D

8. *(a)* In an amplitude modulation process, the carrier and modulating signals, respectively, are

$$e_c = E_c \sin \omega_c t$$

$$e_m = E_m \sin \omega_m t + \frac{E_m}{2} \sin 2\omega_m t + \frac{E_m}{3} \sin 3\omega_m t + \frac{E_m}{4} \sin 4\omega_m t$$

Derive an expression to show that for every modulating frequency component, the AM wave contains two sideband frequencies in addition to the carrier. Draw the frequency spectrum of this AM signal. Also find the value of composite modulation index. 14

(b) Explain the advantages and disadvantages of digital communication over analog communication. 10

(c) A 25 MHz carrier is modulated by a 400 Hz audio sine wave. If the carrier voltage is 4 V and the maximum frequency deviation is 10 kHz, obtain the equation of frequency-modulated wave. Now, if the modulating frequency is changed to 2 kHz, keeping all other parameters same, write the new equation of FM wave. 8

(d) Explain the need of synchronizing pulses in TV. Also mention the basis for deciding the synchronizing frequencies. 8

9. (a) A three-phase, half-wave rectifier is operating from a three-phase, star-connected supply of 220 volts, 50 Hz. The load resistance at the d.c. terminals of the rectifier is 10 ohms. At 75% of the maximum d.c. output voltage, calculate *(i)* the firing angle of SCR, *(ii)* average and r.m.s. load currents, and *(iii)* rectifier efficiency. 15

(b) *(i)* For a single pulse-width modulation of a single-phase inverter, what is the distortion factor for pulse width of $\frac{\pi}{2}$? 5

(ii) A single-phase, half-bridge inverter is feeding power into a load of resistance 10 ohms; d.c. input to the inverter is 400 V. Determine the r.m.s. load voltage, load current and power factor. 10

(c) A step-down d.c. chopper has load resistance of 20 ohms. Chopper input voltage is 200 V d.c. The chopper switch has a voltage drop of 1·5 V when conducting. If the chopper frequency is 2 kHz, find the input and output power of the chopper at a duty cycle of 0·5. Also find chopper efficiency. 10

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