A-GTD-O-FDBB

ELECTRICAL ENGINEERING

Paper II

(Conventional)

Time Allowed : Three Hours *Maximum Marks : 200*

INSTRUCTIONS

Please read each of the following instructions carefully before attempting the questions :

Candidates should attempt FIVE questions in all.

Question No.1 is compulsory.

Out of the remaining SIX questions, attempt any FOUR questions.

All questions carry equal marks. The number of marks carried by a part/question is indicated against it.

Answers must be written in ENGLISH only.

Unless otherwise mentioned, symbols and notations have their usual standard meanings.

Assume suitable data, if necessary, and indicate the same clearly.

Neat sketches may be drawn, wherever required.

All parts and sub-parts of a question are to be attempted together in the answer book.

Attempts of questions shall be counted in chronological order. Unless struck off, attempt of a question shall be counted even if attempted partly.

Any page or portion of the page left blank in the answer book must be clearly struck off.

1. (a) A 37·3 kW dc motor has a full load speed of 1145 rpm. The armature current at full load is 75 A and the friction, windage and core-losses are 8000 W. If the flux in each pole of the motor is reduced to 60% of its rated value and armature current is 75 A, what is the electromagnetic torque developed by the motor ? *4*

(b) In a 4-pole, 50 Hz single-phase induction motor, the power absorbed by the forward and backward fields are respectively 200 W and 21 W at a motor speed of 1440 rpm. The no-load rotational loss is 41 W. Compute the shaft torque at the above speed. *4*

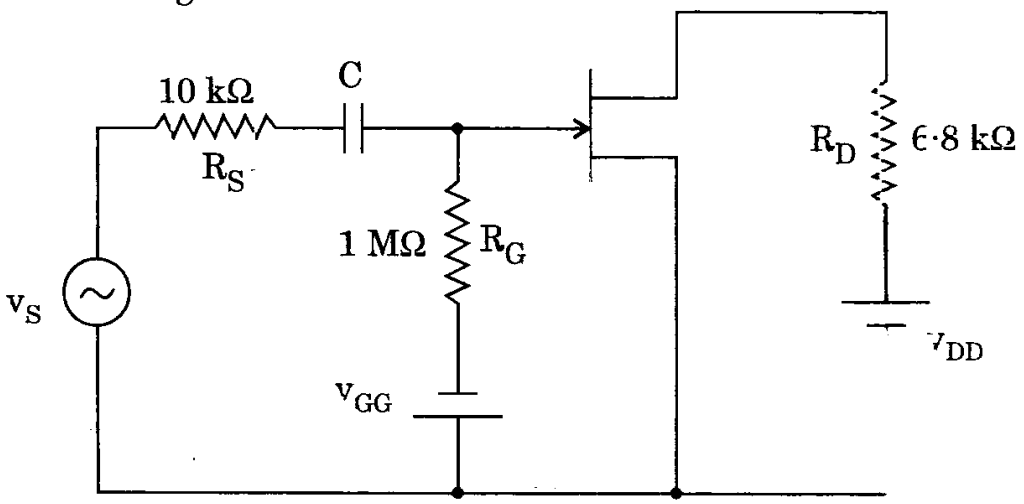
(c) (i) Compare point-to-point HVDC links and back-to-back HVDC links and mention their applications.

(ii) Distinguish between unit commitment and economic load dispatch. *2+2*

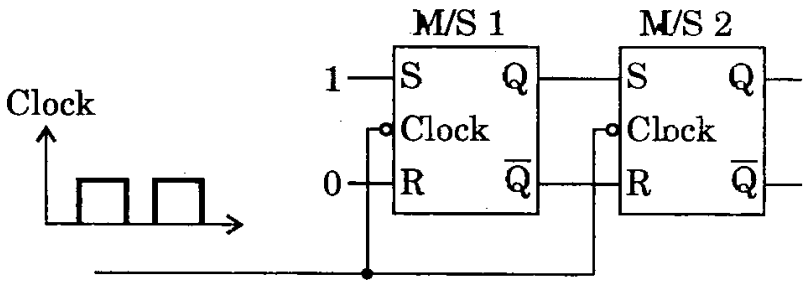
(d) (i) What do you understand by infinite line and infinite bus ?

(ii) Discuss the physical significance of Surge Impedance and Surge Impedance Loading ? *2+2*

(e) The parameters of FET used in the amplifier given below are g_m = 4 mΩ and r_d = 30 kΩ. Assuming C to be a short circuit for the given frequency, determine the small signal voltage gain. 4



(f) The following figure shows two master-slave RS flip-flops having a common clock input. Construct a timing diagram showing the responses of master and slave latches in each flip-flop to two clock pulses. Assume all latches are initially reset. 4



(g) Write the different modes of 8253 IC. 4

(h) What are the limitations of the first order PLL for FM demodulation ? Explain how this is overcome in second order PLL. *4*

(i) Derive an expression for r.m.s. output voltage of a 1-phase AC voltage controller feeding an R-L load. Draw the circuit and waveforms. *4*

(j) A dc motor is fed from a 220 V DC supply through a chopper circuit operating on constant chopping frequency of 800 Hz. The armature and series field resistances are 0·08 Ω and 0·04 Ω respectively. The back emf of the motor is 170 V. Find the ON and OFF periods of the chopper. Assume armature current is 50 A. *4*

2. (a) A transformer has a maximum efficiency of 98% at 3/4th of its full load at unity p.f. The iron losses equal 314 watts. Compute the efficiency of the transformer at 50% and 100% rated full load at the same power factor. *10*

(b) A 1000 MW control area-1 is interconnected with control area-2. The 1000 MW area has the system parameters as follows :

$$R = 2 \text{ Hz/p.u. MW}$$

Damping coefficient = 0·01 p.u. MW/Hz and $\Delta P_{D_1} = 0{\cdot}01$ p.u. MW.

Area-2 has the same parameters of the 5000 MW base. Compute the static frequency drop and static tie-line power. Consider 5000 MW as base. *10*

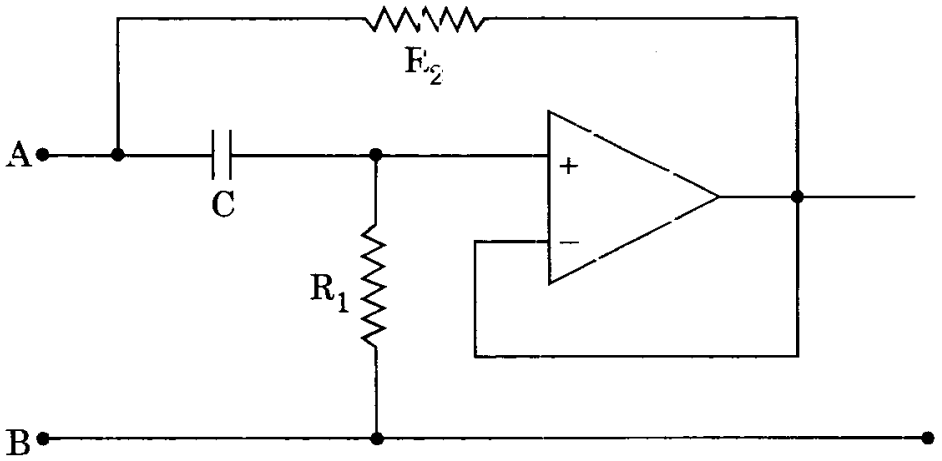
(c) A 1-quadrant chopper feeds an RL load comprising a resistance of 10 ohms and an inductance of 15 mH and is fed from a 110 V dc. Determine the (i) minimum and maximum values of load current (ii) peak-to-peak ripple (iii) average value of load current. Assume chopper frequency is 500 Hz, duty cycle = 0·5 and current is continuous. *10*

(d) Why is TDM superior to FDM in PAM system ? Draw the circuit diagram of a PWM modulator using 555 timer. *5+5*

3. (a) A 3-phase, 4-pole alternator is to be synchronized to an infinite bus of frequency 50 Hz. Three synchronizing lamps L_1, L_2 and L_3 are connected between the phases RYB and RBY of the alternator and the bus bar respectively. Determine the sequence in which the lamps will become dark and the frequency of lamps becoming dark if the speed of incoming generator is (i) 1490 rpm (ii) 1510 rpm. In which case synchronizing switch should be closed and why ? *15*

(b) A single-phase ac regulator is used to control the power output of a heater. The supply voltage is 220 V, 50 Hz and the resistance of the heater is 100 Ω. If the regulator is operated at a firing angle (α) of 90°, draw the voltage waveform across the regulator. Derive the expression for input p.f., power output and input current and determine their values. *10*

(c) The following circuit is used for simulation of inductance by OP-AMP :



Show that we can have a tuned circuit, if we connect a capacitance between A and B and the maximum Q of the inductance is obtained when $\omega = \frac{1}{C\sqrt{R_1 R_2}}$. *10+5*

4. (a) A single-phase fully controlled bridge converter is used to control the speed of a separately excited dc motor. A reactor of 50 mH is connected in the armature circuit. The converter is connected to 220 V, 50 Hz supply and is operated at a firing angle (α) of 90°. The back emf of the motor is 180 V. Draw the output voltage waveform of the converter and determine the peak value of current drawn. Neglect the resistance and reactance of dc machine armature. *15*

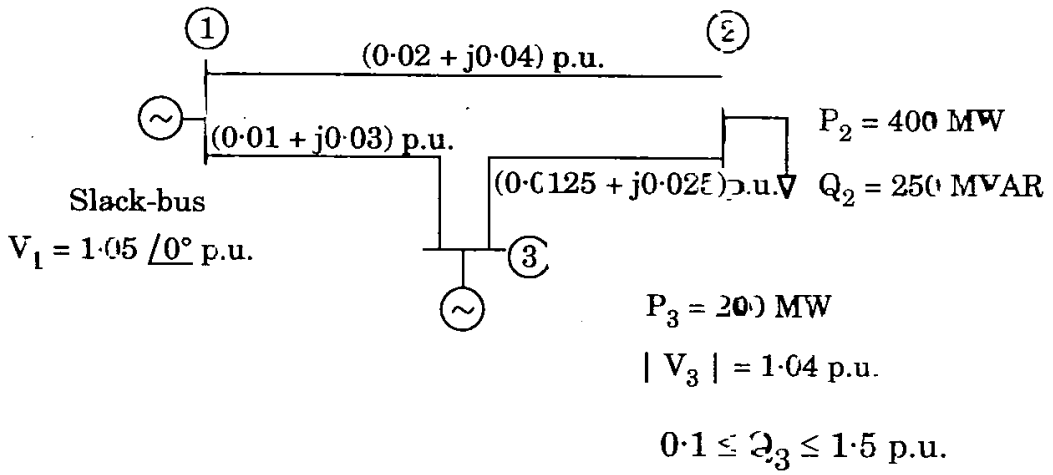
(b) A power system to which a generator is to be connected at a certain bus may be represented by the Thevenin's voltage $E_{th} = 0{\cdot}9 \angle 0°$ p.u. in series with $Z_{th} = 0{\cdot}25 \angle 90°$ p.u. When connected to the system, E_g of the generator is $1{\cdot}4 \angle 30°$ p.u. Synchronous reactance of the generator on the system base is 1·0 p.u.

(i) Find the bus voltage V_t and real power (P) and reactive power (Q) transferred to the system at the bus.

(ii) If the bus voltage is to be raised to $|V_t| = 1{\cdot}0$ p.u. for the same P transferred to the system, find the value of E_g required and the value of Q transferred to the system at the same bus. Assume all the other system emf's are unchanged in magnitude and angle, that is, Thevenin's voltage and impedance are constant. *15*

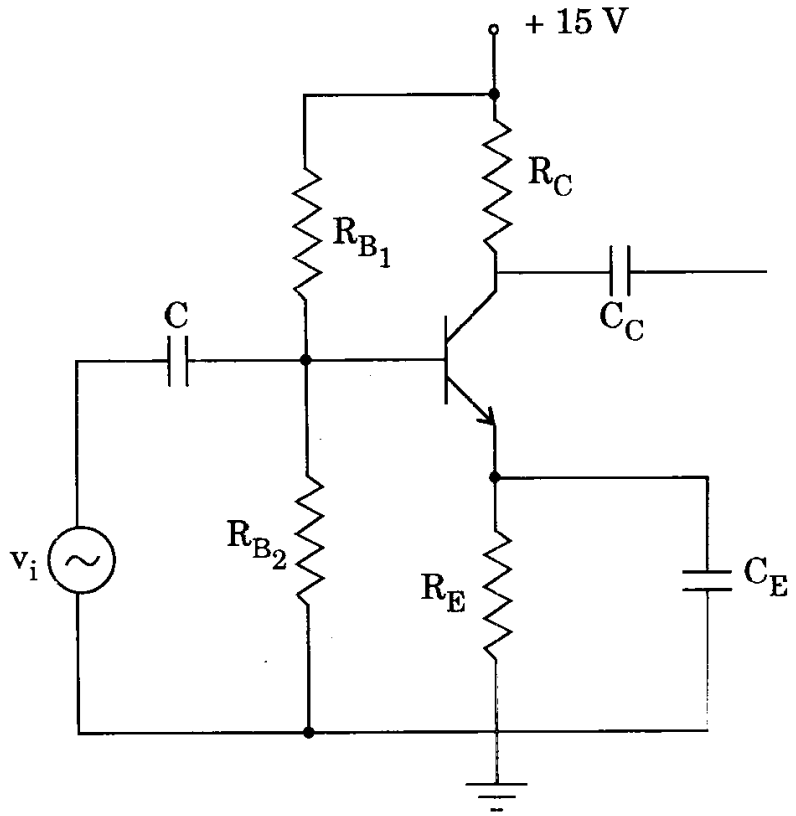
(c) Draw a logic diagram showing how four exclusive-OR gates, four AND gates and two OR gates can be connected to construct a 2-bit parallel adder. 15

5. (a) The figure shows single line diagram of a power system with generators at buses 1 and 3. The voltage at bus-1 is $1{\cdot}05 \angle 0°$ p.u. and at bus-3, $|V| = 1{\cdot}04$ p.u. Line impedances are in p.u and the line charging susceptances are neglected. Obtain the state vector after one iteration using Fast Decoupled Load Flow. 15



(b) The following circuit is used as a CE amplifier employing potential divider bias. If $h_{fe} = 50$ and $v_{BE} = 0{\cdot}6$ V, determine the values of R_C, R_E, R_{B_1} and R_{B_2} for quiescent operating $I_C = 1$ mA and $v_{CE} = 7{\cdot}5$ V.

Assume $R_B = R_{B_1} \parallel R_{B_2} = 10\ R_E$. *15*

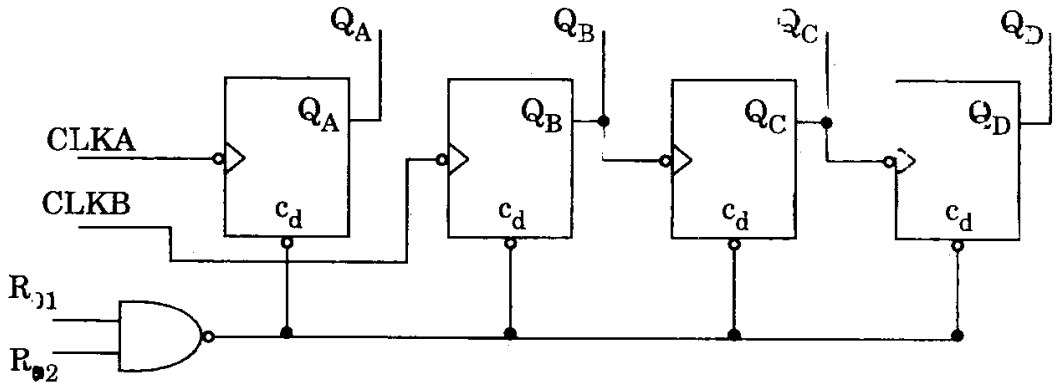


(c) A manufacturing plant uses 100 kVA at 0·6 p.f. lagging under normal operation. A synchronous motor is added to the system to improve the overall power factor. The power required by the synchronous motor is 10 kW. Determine the overall power factor when the synchronous motor operates at 0·5 p.f. leading. What must be the power factor of the motor to improve the overall power factor to 0·9 lagging ? *15*

6. (a) A three-phase power system consists of a synchronous machine connected through a lossless double circuit transmission line to an infinite bus-bar. A fault occurs on the transmission line. The maximum power transfer to this system is 5·0 p.u. during pre-fault condition and immediately prior to the instant of the fault, the power transfer is 2·5 p.u. The power angle curves during the fault and post-fault conditions have peak values of 2 p.u. and 4 p.u. respectively. Determine the permissible increase in the angular displacement, between the voltages at the two ends of the system beyond which the circuit breakers could not clear the fault in time for the system to remain in synchronism. *10*

(b) A 1-phase bridge inverter is feeding an R-L load with R = 8 Ω, L = 0·04 H. Find the load voltage and current expressions for the first two half cycles with rectangular wave output at 50 Hz The input to the inverter is 220 V. *10*

(c) Show how the counter shown in the following figure can be configured to operate as a mod-12 counter : *10*



(d) Two synchronous generators are operating in parallel and supplying a load of 2·5 MW at 0·8 pF lagging. Generator '1' has a no-load frequency of 51·5 Hz and a slope (S_{P_1}) of 1 MW/Hz. Generator '2' has a no-load frequency of 51 Hz and a slope (S_{P_2}) of 0·8 MW/Hz.

(i) At what frequency is this system operating, and how much power is shared by each of the two generators ?

(ii) What will be the system frequency and generated powers, if the governor set point on G_2 is increased by 0·5 Hz ?

(iii) How can the load be transferred from Generator '1' to Generator '2' without changing the system frequency ? *10*

7. (a) The single area control system shown in the figure has the following data :

$T_p = 10$ sec

$T_g = T_t = 0$

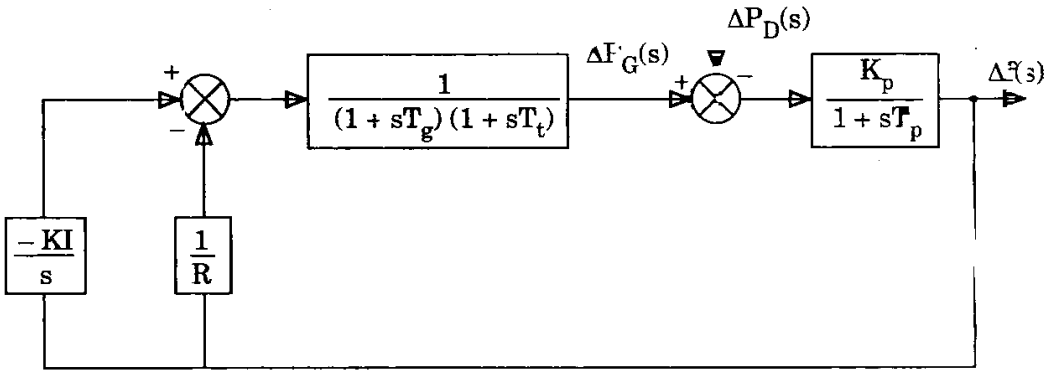
$K_p = 100$ Hz/p.u. MW

$R = 3$ Hz/p.u. MW

$\Delta P_D = 0{\cdot}1$ p.u. MW

$K_I = 0{\cdot}1$

Compute the error caused by the step disturbance of magnitude given above. Prove that the error is reduced by increasing the given K_I. Express the error in seconds and cycles, if the system frequency is 50 Hz. *10*



(b) What type of data transfer schemes are used when there is a speed mismatch between microprocessor and I/O devices ? Explain cycle stealing technique. *10*

(c) (i) How is charge stored in an EPROM cell ? How is it removed ? Briefly describe the mechanisms involved.

(ii) A 128 K × 8 memory is to be constructed using 16 K × 8 circuits each of which has an active-low chip-select input. Draw a logic diagram showing only the connections necessary for the chip-select inputs. It is not necessary to show address or data pins on the individual 16 K × 8 circuits. *4+6*

(d) Differentiate between type tests and routine tests. What are the different tests carried out to prove the ability of circuit breaker ? *10*
