2007 CALICUT UNIVERSITY

III SEMESTER B.TECH COMPUTER SCIENCE & NGINEERING

SWITHCHING THEORY AND LOGIC DESIGN

JUNE 2007

TIME::3 HOUR
MARK:100

ANSWER ANY TEN QUESTIONS QUESTIONS CARRY EQUAL MARKS

MARKS [10*10=100]

1. What do you mean by swithching algebra?

2. Explain why NAND gate is known Y=AB+A+B and draw the logic circuit

3. Explain why NAND gate is known as universal gate.

4. Implement a 4:1 multiplexer.

5. Write a brief note on fault classes.

6. Write short notes on PLA folding.

7. Give the excitation tables of JK and D flipflop

8. Explain the basic concepts of a shift register.

9. Reduce the following Boolean function using mccluuskey method
F(A,B,C,D,E)=SUM(0,1,2,8,9,15,17,21,24,25,27,31)

10. Simplify the following expression using K-map
F(A,B,C,D)=SUM(0,3,6,7,9,13,14,15)

11. Differentiate between normal and cannonical forms with the help of suitable examples.

12. implment a bcd to excess 3 converotr.

13. Explain the difference between multiplexer and demultiplexer with the help of neat logic diagrams.

14. Discuss about the fault table method for test generation.

15. Write short notes on the following:-

Essential prime cube theorem.
Design for testability.

16. Design a 4-bit up down counter and explain.

17. What do you mean by synchronous counters? Design a mod-8 sychronous binary up counter using D Flip flop.